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# Standardized Test Routines for the Assessment of Potential Induced Degradation of Perovskite Solar Cells


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## ABSTRACT

Potential induced degradation (PID) is well-understood in crystalline silicon solar cells and is commonly caused by sodium ions creating shunts. Standard PID tests have been developed for these conventional cells. Our investigation looked into whether standardized PID tests are suitable for perovskite solar cells of various architectures and compositions. We discovered that these tests could reveal the PID resistance of such cells. Despite perovskite materials' distinct differences from silicon-based cells, PID testing shows their PID resistance capability, vital for developing photovoltaic (PV) modules.


## MATERIALS AND METHODS

### *Sample Details*

We have two different sample sets from Fraunhofer ISE (Sample Set A) and Saule Technologies (Sample Set B), and we wanted to tackle **whether standardized testing predicts the long-term stability of perovskite modules even though their compositions and structures vastly differ.**

(a) (b) (c)

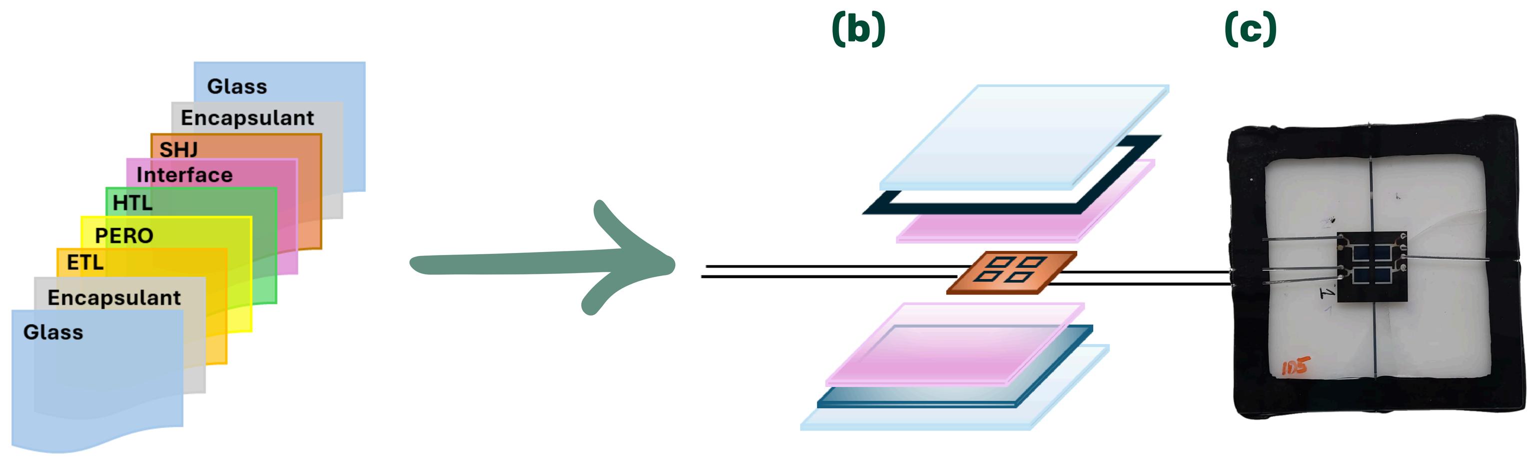


*Figure 1. Schematics showing (a) the layers of perovskite silicon tandem modules (from ISE) with the top cell being perovskite and the bottom cell made of silicon heterojunction, (b) the encapsulation structure of the modules, and (c) an actual picture of the module.*

(a) (b)

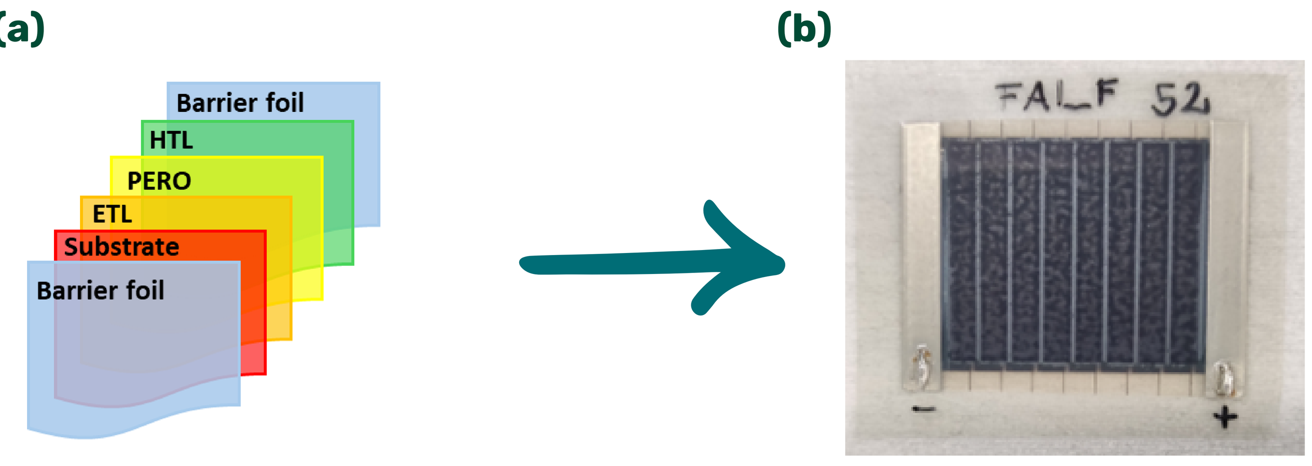


*Figure 2. A schematic showing (a) the layers of perovskite modules (from Saule), (b) an actual picture of the module.*

### *Measurement Method*

In this study, we utilized the PIDcon Bifacial device, developed in Freiburg Instruments, to conduct the PID tests and the Sinus 220 Wavelabs Instrument for electrical characterization. Table 1 presents the technical specifications of the PIDcon Bifacial, and Fig. 3 shows the test sequence.

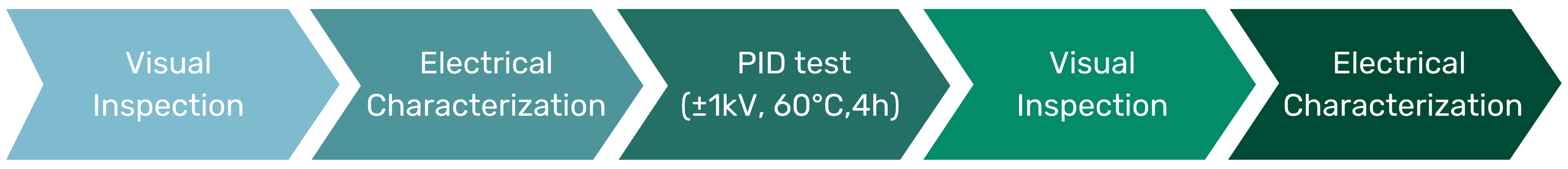


*Figure 3. The testing sequence diagram.*

| Technical Specifications | |
|---|---|
| Dimensions (W x H x D) | 310 x 340 x 275 mm |
| Electrode (100 x 100 mm) | 0.1 to 1.5 kV |
| Temperature | Up to 150°C |
| Measurement Time | Minutes to days |
| Measured Parameters | Measured voltage [mV], measured current [mA], parallel resistance [Ω], conductance, humidity [%], leakage current [µA], power loss [%] |

*Table 1. Technical specifications of the PIDcon Bifacial device.*

## RESULTS

We comprehensively conducted and evaluated the J-V measurements (reverse scan, scan range depends on the sample parameters) of two sample sets at three stages: initially, after 1 hour of PID testing, and after three more hours of PID testing. The values are normalized to Voc and Isc of the samples.

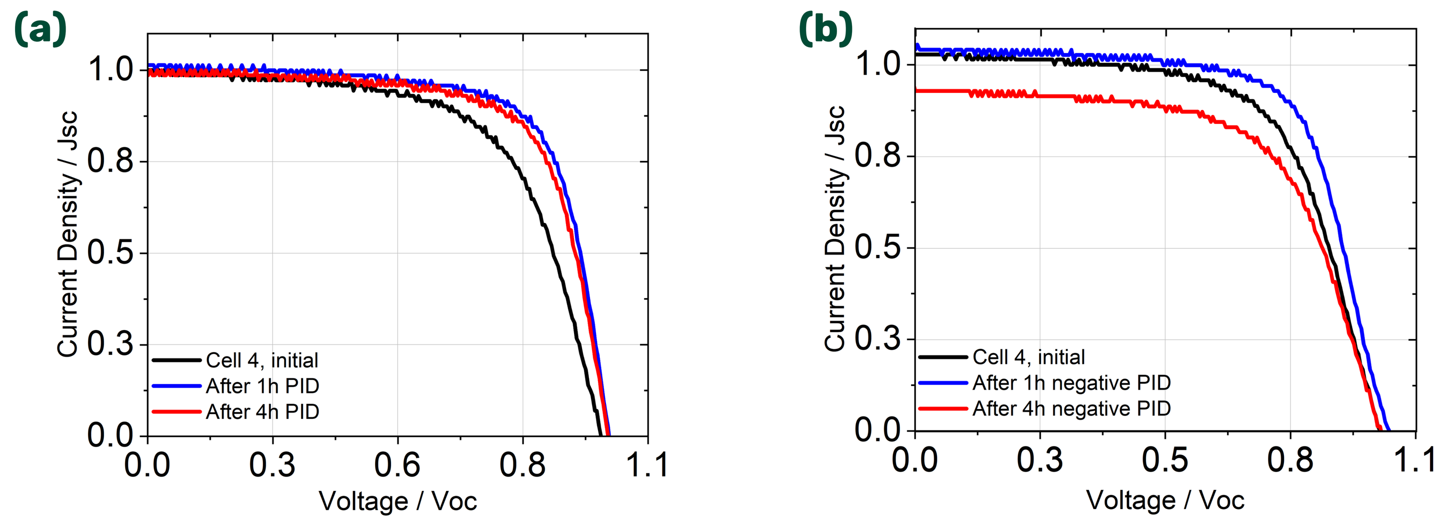


*Figure 4. J-V curves of (a) cell_4 on a Pero-Si-Tandem module under positive PID stress (1kV, 60°C), (b) cell_4 on the same module under negative PID stress (-1 kV, 60°C). The samples were stored in a dark nitrogen box between PID tests with varying voltage bias polarity.*

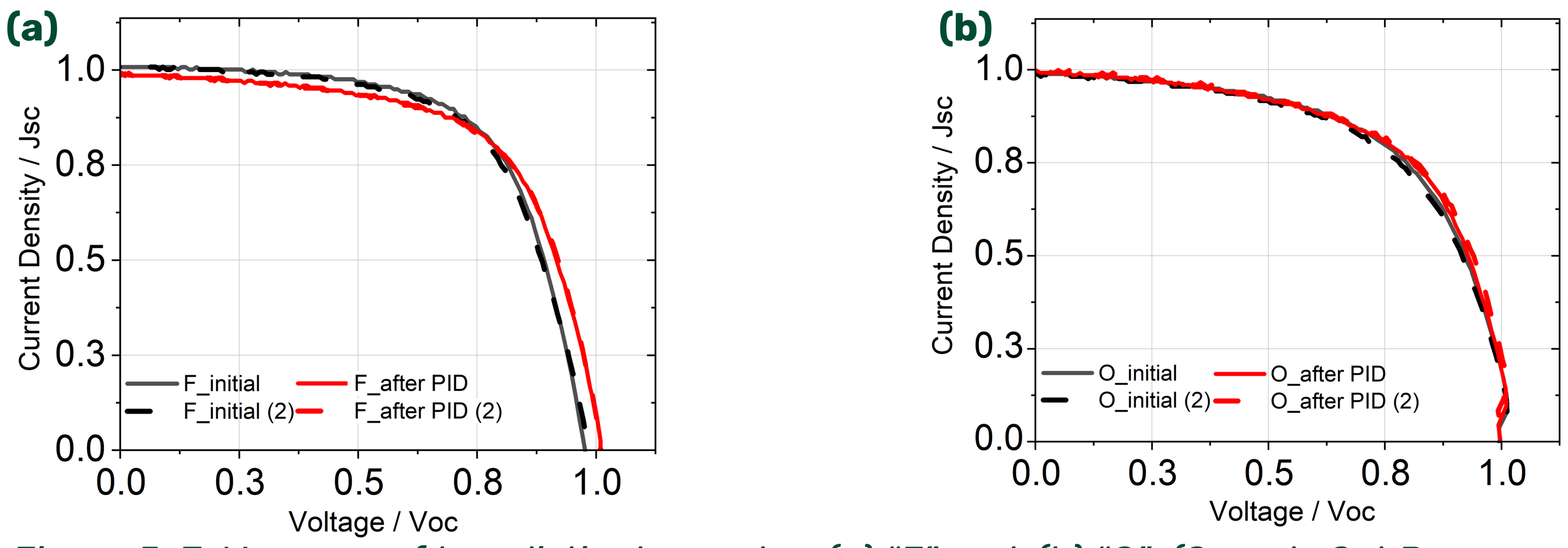


*Figure 5. J-V curves of two distinct samples, (a) "F" and (b) "O" (Sample Set B, different precursor composition), before and after PID testing (1 kV, 60°C, 4h).*

| | FF_initial | | FF_after |
|---|---|---|---|
| 1KV, 60°C | 63.3% | → | **69.3%** |
| -1 KV, 60°C | 63.0% | → | **62.5%** |

Cells exhibited a notable rise in FF after the initial hour of PID testing, regardless of the voltage bias polarity. **Positive PID** testing **maintained high FF levels** over an additional three hours, but **negative PID** testing **slightly lowered FF values.**

Before PID testing, sample type "F" exhibited an average FF of 64.0%. After PID testing, **FF showed a slight decrease of approximately 1.1%**, and **Voc exhibited an increase of approximately 2.6%.** Sample type "O" demonstrated a **notable FF increase of around 2.5%** after PID testing.

Our study successfully applied standardized PID testing to perovskite solar cells, revealing a range of responses to stress conditions. We managed to distinguish between **temperature-induced** and **voltage-induced** effects by varying the polarity of voltage bias. While some samples exhibited minimal degradation, others showed performance improvements, which can more certainly be attributed to the high temperature than the applied external voltage. These findings underscore the need for further research to optimize testing methodologies and mitigate potential degradation mechanisms in PSCs.


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